piesimaging

EPFL's spin-off company Michel Antolovic

Mission: to change the way we count photons

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Enabling innovation in microscopy





Detector technology: CMOS SPAD



• SPAD/APD chip (+ readout electronics and sample software)



SPAD image sensors



• Unprecedented image quality at low light, high video rate



<u>156 fps</u> <u>2604 fps</u> <u>15625 fps</u> Download full videos



Kazuhiro Morimoto *et al,* 2020

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Protected technology – single-photon avalanche diode (SPAD)



- 3 patent applications exclusively licensed to Pi Imaging
- 3 joint patent applications
- Limited number of production facilities capable of producing high quality CMOS SPADs
- SPAD design kept as trade secret





EU project



- Objectives:
 - Tailor the existing detector for MINFLUX microscopes
 - Develop novel SPAD arrays with enhanced red and NIR sensitivity
 - Develop a 10×10 SPAD array with time-gating
- Contribution in the project:
 - Provide direct photon information to the microscopy platform, improve spatial and temporal resolution
 - Improve red and NIR detection

Work package 3



• Task 3.1: Gen I detection electronics

- The Gen I detection electronics will forward software-selectable SPAD array channels with intrinsic jitter through a reconfigurable FPGA. SPAD channels are going to be forwarded to 4 input channels available in the MINFLUX system.
- **Deliverable:** Two SPAD arrays integrated, tested and delivered to AI for integration (M6).

• Task 3.2: Gen II detection electronics

- Photon counting/time-tagging and microscope control will be merged through a dedicated communication protocol. This will enable utilization of all 23 pixels of the SPAD array with 20 ps timing resolution.
- **Deliverable**: Upgrade to Gen II detection electronics with time-tagging and 20 ps timing resolution (M30).

Work package 3 (II)



- Task 3.3: Enhanced red and NIR sensitivity CMOS SPAD
 - PII will develop SPAD arrays with enhanced red and NIR sensitivity, targeting a peak quantum efficiency (QE) above 50% at 640 nm and specially enhanced QE spectra between 600 nm and 900 nm. The array will be optimized for off-chip time-gating, with a timing jitter of less than 250 ps at 640 nm.
 - **Deliverable**: Replace SPAD arrays with newly designed CMOS SPAD array with enhanced red and NIR sensitivity (M32).
- Task 3.4: 10×10 CMOS SPAD array with integrated time-gating
 - Small image sensors with 1 Mframes per second and chip-level time-gating with 1 ns gate
 - Deliverable: Characterization of 10×10 CMOS SPAD array (M36)

Gen I detection electronics



- Working plan for the first 6 months:
 - Update software and firmware to pass SPAD pulses from programmable pixels to 4 SMA outputs



Gen II detection electronics



- Working plan for the first 6 months:
 - Determine the hardware platform (FPGA system+connections) for the interface between the detector and the microscope
 - Define a communication protocol (bidirectional high speed, unidirectional high speed)





Enhanced red and NIR sensitivity CMOS SPAD



- Working plan for the first 6 months:
 - Evaluate 5 versions of the red SPAD in terms of fill factor and noise (crosstalk)



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